REMARKS

Claims 1-31 are all the claims pending in the application.

Summary of the Office Action

The Examiner withdrew the previous grounds of rejection. The Examiner, however, found new grounds for rejecting some of the claims. In particular, claims 2, 10, 14, 18, and 21-23 are allowed and claims 3-9, 11, and 12 contain allowable subject matter.

Claim rejection under 35 U.S.C. § 112, first paragraph.

Claims 13, 27, and 28 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Examiner states that "Applicant is claiming, 'A computer -readable medium', which is not discussed in the specification." Applicants traverse the rejection for at least the following reason.

Applicants respectfully submits that MPEP section 2164 states:

> The purpose of the requirement that the specification describe the invention in such terms that one skilled in the art can make and use the claimed invention is to ensure that the invention is communicated to the interested public in a meaningful way. The information contained in the disclosure of an application must be sufficient to inform those skilled in the relevant art how to both make and use the claimed invention.

Applicants respectfully submit that page 10, lines 27-30 describes that "[t]he compensation module according to the invention can also be implemented as a software module or program module whose program code can be executed by a suitable control means, for example a digital signal processor." Applicants respectfully submit that it is well known to one skilled in the art at the time the invention was made that software modules and program modules are stored on

computer readable mediums. Unless the program is stored on some form of a computer readable medium, it cannot be executed. As such, it would have been quite clear to one of ordinary skill in the art that the software module or program module which may implement a compensation module would be stored on a computer readable medium. Therefore, the information contained in the disclosure of an application is sufficient to inform those skilled in the relevant art how to both make and use the claimed invention.

Furthermore, MPEP section 2181 states:

> In considering whether there is 35 U.S.C. 112, first paragraph support for the claim limitation, the examiner must consider not only the original disclosure contained in the summary and detailed description of the invention portions of the specification, **but also the original claims**, abstract, and drawings. See In re Mott, 539 F.2d 1291, 1299, 190 USPQ 536, 542-43 (CCPA 1976) (claims); In re Anderson, 471 F.2d 1237, 1240, 176 USPQ 331, 333 (CCPA 1973) (claims).

Applicants respectfully submit that the original claim 13 recites "A memory means, in particular a floppy disc, CD-ROM, digital versatile disc, hard disc-drive or the like, with a compensation module according to Claim 12 stored thereon." (See, for example, page 27, lines 10-12 of the original disclosure.)

Applicants respectfully submit that since the original claim provides some examples of the memory *i.e.*, computer readable medium, that could be used to store the compensation module, one of ordinary skill in the art would be enabled to make and use the invention as recited in claim 13.

In view of the above, Applicants submit that the feature of 'a computer-readable medium' is described in the original disclosure in such a way as to enable one skilled in the art to use and make the invention. Thus, Applicants respectfully request the Examiner to withdraw the rejection of claims 13, 27 and 28 under 35 U.S.C. § 112, first paragraph.

Claim rejection under 35 U.S.C. § 103

Claims 1, 13, 15-17, 19, 20 and 24-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hamamoto et al. (US Patent No. 5,987,619) in view of Hillis et al. (US Patent No. 5,118,975). Applicants traverse the rejection for at least the following reasons.

The Examiner alleges that "it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of a first delay means as [allegedly] taught by Hillis with the teachings Hamamoto for the purpose of further providing reliable data communication with the managing timing associated with the communication signaling" (*see* page 4 of the Office Action).

Applicants respectfully submit that MPEP section 2143.01 states:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Hamamoto is directed to a circuit for compensating a phase in data input to the semiconductor memory. Applicant respectfully submits that Hamamoto discloses that two signals FCLK and BCLK will have different phases, as explained in greater detail below.

Specifically, Hamamoto discloses that two variable delay circuits 5 are controlled by a phase comparator 29. The delay circuits 5 receive FCLK and BCLK signals, respectively that are generated by the clock signal generation circuit 7. The clock signals FCLK and BCLK are generated such that BCLK is phase shifted by 180 degrees from the clock signal FCLK. These clock signals FCLK and BCLK are input into corresponding variable delay circuits 5 and delayed by a common time Dv (column 6, lines 25-34).

Applicants respectfully submit that the principle feature of the clock signal generation circuit of Hamamoto is to generate FCLK and BCLK that are phase shifted by 180 degrees. However, if one skilled in the art were to modify this feature by phase adjusting BCLK (alleged the second delay means), so that BCLK (the alleged delayed second clock signal) is adapted to the phase of FCLK (the alleged delayed first clock signal) the principle of operation of the feature disclosed in Hamamoto will be modified. That is, instead of generating FCLK and BCLK being out of phase by 180 degrees, which is the principle of operation of the feature, the FCLK and BCLK would be in phase modifying the principle operation of Hamamoto. As such, Applicants respectfully submit that it is improper for the Examiner to allege that it would have been obvious to one skilled in the art to combine the teaching of Hamamoto and Hillis.

Second, Applicants submit that even if, *assuming arguendo*, the teachings of Hamamoto and Hillis are combined as asserted by the Examiner, the result of the combination would not disclose all the features of claim 1.

Claim 1, recites, *inter alia*, "adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of the first delay means." The Examiner admits that Hamamoto fails to disclose the unique feature of claim 1 described above. However, the Examiner alleges that Hillis supplies the features missing in Hamamoto (*see* page 4 of the Office Action). Applicants respectfully disagree with the Examiner for at least the following reason.

Hillis is directed to a clock buffer control circuit for controlling relative timing of sequential ticks of a clock signal used to control the digital circuitry (column 1, lines 6-10). Hillis discloses that the clock buffer circuit generates a local clock signal in response to a system clock signal. The clock buffer circuit controls the relative phases of the clock signal in relation to the system clock signal (column 2, lines 4-6). However, Hillis does not disclose an adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of the first delay means.

In particular, Hillis discloses a phase comparator 23 which indicates a selected timing relationship between the SYS CLK IN system clock and the DEL CLK OUT REF delayed clock out reference signal. The response that is generated can be a LEAD signal, a LAG signal, a PH OK in-phase signal and a PH BAD out-of-phase signal. The PH-OK in-phase signal indicates

that the edges of the system clock occur substantially simultaneously with the edges of the delayed clock out reference signal (column 4, lines 40-64). Applicants submit that it is quite clear from the above, Hillis discloses comparing a system clock signal and delayed signal and does not disclose a first delayed signal and second delayed signal. That is, Hillis disclose only one delayed signal and does not disclose a first and second delayed signal.

Furthermore, Applicants submit that Hillis merely discloses that the PH OK in-phase is used by delay control circuit 22 in controlling the variable delay element 20 and does not disclose the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of the first delay means. Particularly, Hillis does not disclose comparison between a first delayed clock signal and a second delayed clock signal. Consequently, Hillis also does not disclose the delayed second clock signal adapted to the phase of the delayed first clock signal. Hamamoto also does not disclose the delayed second clock signal being adapted to the phase of the delayed first clock signal.

In view of the above, Applicants submit that Hamamoto and Hillis, alone or in combination, do not disclose "adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of the first delay means." Thus, Applicants respectfully request the Examiner to withdraw the rejection of claim 1.

Claims 13 and 15

Independent claims 13 and 15 recites features similar to the features argued above with respect to claim 1. Therefore, arguments presented with respect to claim 1 are respectfully

submitted to apply with equal force here. For at least substantially analogous exemplary reasons, therefore, independent claims 13 and 15 are patentably distinguishable from Hamamoto and Hillis.

Claims 16, 17, 19, 20, and 24-31

Applicants submit that claims 16, 17, 19, 20, 24, and 26 are patentable by virtue of their dependency on claim 1 or 15.

Allowable Subject Matter

Applicants thank the Examiner for allowing claims 2, 10, 14, 18, and 21-23. Applicants further thank the Examiner for indicating that claims 3-9, 11, and 12 contain allowable subject matter. Applicants do not acquiesce to the Examiner's Reasons for allowance. Also, Applicants respectfully hold the rewriting of these claims in abeyance until arguments presented with respect to the independent claims have been reconsidered.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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